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EXAMINER	
HSU, JONI	

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2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/622,417	MAS ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 30-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *30-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 7-9, filed January 9, 2008, with respect to Claims 1, 2, 4, and 5 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections of Claims 1, 2, 4, and 5 have been withdrawn.

2. Applicant's arguments filed January 9, 2008, with respect to Claims 30-45 have been fully considered but they are not persuasive.

3. Applicant argues that Miyachi (US006937224B1) do not mention shifting storage locations within memory, such as holding memory 3. Cited passages of Miyachi do not mention memory, but rather describe activation of row/column line drivers to display image (p. 9-10).

In reply, Examiner points out Fig. 3 of Miyachi shows selector switch 35 is placed at preceding stage of holding memory. Selector switch receives switching clock signal and selects black signal data derived from black signal data generating section 36 and transmits data to holding memory (c. 12, ll. 45-57). Since row line is being shifted based on selecting black image display signal (c. 5, ll. 50-58; c. 6, ll. 1-7; c. 1, ll. 12-20; c. 3, ll. 46-c. 4, ll. 7), and black signal data is selected prior to transmitting data to holding memory (c. 12, ll. 45-57), this means storage locations within holding memory are in fact being shifted.

4. Applicant argues Choi (US 20030076332A1) contains no mention of address, much less performing operation on first address to determine second address. Office Action assumes operation unit 105 uses addresses to access memory 102 and performs operation on addresses to move image. Fig. 1 of Choi shows operation unit 105 of Choi is not connected to memory 102. Rather, image is written to and read from memory 102 by signal processor 101. Operation unit

105 operates on display unit to display image in desired position, based on control signal from controller 104. Operation unit 105 moves image by operating display unit, not by performing calculations on addresses to obtain new addresses (pages 10-11).

In reply, Claims 42-45 do not expressly recite addresses are memory addresses. Claim 42 recites "shifting a position at which an image is to be displayed". So, "address" could be interpreted to be display address; this is the way "address" is being interpreted in this rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 30, 35, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyachi (US006937224B1).

7. As per Claim 30, Miyachi teaches supplying select signal to nth row line and also supplying data signal to column lines, thereby displaying image to pixels located at intersecting points between nth row line and individual column lines (c. 3, ll. 58-63); and then iterating display operation based on data signal (shifting the column) while sequentially shifting row line to which select signal is supplied (c. 4, ll. 4-7), which causes position of displayed image to be shifted. So, Miyachi teaches circuit for shifting position at which image is to be displayed, image being represented by image data comprising plurality of rows and plurality of columns corresponding to pixels of image (c. 3, ll. 58-63; c. 4, ll. 4-7), circuit comprising first memory

(sampling memory 2, Fig. 31) that stores image data; second memory (holding memory 3) that receives row of image data from first memory (2) and stores row of image data at first storage locations of second memory (3) (c. 1, ll. 12-20); and control circuit (display control section) that provides column offset value to second memory (3); wherein second memory (3) shifts storage locations at which row of image data is stored based on column offset value such that row of image data is stored in second storage locations of second memory (3), second storage locations being shifted with respect to first storage locations (c. 5, ll. 50-58; c. 6, ll. 1-7; c. 1, ll. 12-20; *supplying the data signal to the column lines, thereby displaying an image based on the data signal to pixels located at intersecting points between the nth row line and the individual column lines, iterating the image display operation based on the data signal while sequentially shifting the row line to which the select signal is supplied*, c. 3, ll. 46-c. 4, ll. 7). Fig. 3 of Miyachi shows selector switch 35 is placed at preceding stage of holding memory. Selector switch receives switching clock signal and selects black signal data derived from black signal data generating section 36 and transmits data to holding memory (c. 12, ll. 45-57). Since row line is being shifted based on selecting black image display signal (c. 5, ll. 50-58; c. 6, ll. 1-7; c. 1, ll. 12-20; c. 3, ll. 46-c. 4, ll. 7), and black signal data is selected prior to transmitting data to holding memory (c. 12, ll. 45-57), this means storage locations within holding memory are being shifted.

8. As per Claim 35, Miyachi teaches a plurality of column drivers (12, Fig. 1) that receive the row of image data from the second memory (holding memory 32, Fig. 2) (c. 12, ll. 22-36).

9. As per Claim 37, Miyachi teaches second storage (holding memory) locations are offset from first storage (sampling memory) locations by column offset value (c. 1, ll. 12-20; c. 3, ll. 46-c. 4, ll. 7; c. 5, ll. 50-58; c. 6, ll. 1-7).

10. Thus, it reasonably appears that Miyachi describes or discloses every element of Claims 30, 35, and 37, and therefore anticipates the claims subject.

11. Claims 42-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi (US0020030076332A1).

12. As per Claim 42, Choi teaches moving image, and movement order of image is set as left, upper, right and lower directions, and image is moved by one pixel in each of the directions [0036]. So, Choi teaches circuit for shifting position at which image is to be displayed, image being represented by image data comprising plurality of rows and plurality of columns corresponding to pixels of image. Circuit comprises first memory (102, Fig. 1) that stores image data [0031]; logic unit (105); and control circuit (104) that provides row offset value to logic unit [0036]. If control circuit judges that same image is displayed for certain period of time, it sends control signal, which causes displayed image to move by one pixel in left direction (row offset value), to logic circuit [0035, 0036]. Logic circuit operates display unit so image signal transmitted can be displayed on desired position of display unit according to control signal transmitted by control circuit [0041]. Since display is shifted after same image is displayed, this means logic unit previously received first row address corresponding to row of image data for image that was previously displayed. So, logic unit receives first row address corresponding to row of image data and performs operation on first row address using row offset value to determine second row address that is offset from first row address.

13. As per Claim 43, Choi discloses that the control circuit (104, Fig. 1) further provides a row address offset direction to the logic unit (105) [0036, 0038].

14. As per Claim 44, Choi teaches position is determined by moving image by one pixel in left direction (row offset value) [0036, 0041]. So, position is determined by adding one pixel in left direction to previous position. So, second row address is determined by adding row offset value to first row address or subtracting row offset value from first row address.

15. As per Claim 45, Choi teaches control circuit provides cyclic succession of row offset values to logic unit [0036-0040].

16. Thus, it reasonably appears that Choi describes or discloses every element of Claims 42-45 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyachi (US006937224B1) in view of Kuwata (US005754157A).

20. As per Claim 31, Miyachi is relied on for teachings for Claim 30. Miyachi teaches column driver reads image data from first memory (sampling memory) (c. 12, ll. 19-25).

However, Miyachi does not explicitly teach first memory has frame memory that stores image data for entire image to be displayed. However, Kuwata teaches column driver reads image data from first memory (32, Fig. 7), and first memory has frame memory that stores image data for entire image to be displayed (c. 13, ll. 53-55; c. 14, ll. 20-45; c. 10, ll. 29-35).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Miyachi so first memory has frame memory that stores image data for entire image because Kuwata teaches this way plurality of scanning lines can be simultaneously selected for driving, which increases speed of driving circuit (c. 1, ll. 62-67; c. 13, ll. 53-55).

21. As per Claim 32, Miyachi teaches data from first memory (sampling memory) is stored into second memory (holding memory) within column driver (c. 12, ll. 19-25), and column driver shifts data (c. 5, ll. 50-58; c. 6, ll. 1-17;c. 3, ll. 46- c. 4, ll. 7).

However, Miyachi does not explicitly teach second memory has register. But, Kuwata teaches data from 1st memory (32, Fig. 7) is stored into second memory (171, Fig. 10) in column driver, and second memory has register (c. 13, ll. 53-55; c. 14, ll. 20-45; c. 10, ll. 29-57).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Miyachi so second memory has register as suggested by Kuwata. It is well-known in the art shift registers are registers in which data can be shifted. Since Miyachi teaches column driver shifts data, it would be obvious to modify column driver of Miyachi so it uses shift register to shift data, as suggested by Kuwata.

22. As per Claim 33, Miyachi does not teach register comprises a shift register. But, Kuwata teaches this (171, Fig. 10; c. 10, ll. 48-50). This would be obvious for reasons for Claim 32.

23. Claims 34, 36, and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyachi (US006937224B1) in view of Choi (US 20030076332A1).

24. As per Claim 34, Miyachi is relied on for teachings for Claim 30. Miyachi teaches providing column offset to second memory (holding memory) (c. 1, ll. 12-20; c. 3, ll. 46-c. 4, ll. 7; c. 5, ll. 50-58; c. 6, ll. 1-7). Miyachi teaches eliminating afterimage (c. 16, ll. 4-7).

However, Miyachi does not explicitly teach providing column offset direction. However, Choi teaches control circuit (104, Fig. 1) provides column offset direction [0037, 0039].

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Miyachi so control circuit provides column offset direction because Choi suggests moving image in different directions is efficient manner of eliminating afterimage [0017-0024], and in order to do this, column offset direction needs to be provided [0037, 0039]. Since Miyachi teaches device that eliminates afterimage, it would be obvious to modify Miyachi with method taught by Choi, since Choi teaches this is efficient way to eliminate the afterimage.

25. As per Claim 36, Miyachi teaches eliminating the afterimage (c. 16, ll. 4-7).

However, Miyachi does not explicitly teach control circuit provides cyclic succession of column offset values to second memory. However, Choi teaches this limitation [0036-0040].

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Miyachi so control circuit provides cyclic succession of column offset values to 2nd memory because Choi suggests this is efficient way to eliminate afterimage [0017-0024].

Since Miyachi teaches device that eliminates afterimage, it would be obvious to modify Miyachi with method taught by Choi, since Choi teaches this is efficient way to eliminate afterimage.

26. As per Claim 38, Miyachi teaches shifting storage locations at which the row of image data is stored (c. 4, ll. 4-7).

But, Miyachi does not teach details of method for shifting rows, including control circuit provides row offset value to logic unit; logic unit receives 1st row address corresponding to row of image data and performs operation on 1st row address using row offset value to determine 2nd row address that is offset from 1st row address. But, Choi teaches this, as discussed for Claim 42.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Miyachi to include method of shifting rows because Choi teaches this is needed so rows are shifted to correct position [0036, 0041].

27. As per Claim 39, Miyachi does not explicitly teach providing row offset direction. However, Choi teaches control circuit (104) provides row offset direction to logic unit (105, Fig. 1) [0036, 0038]. This would be obvious for the same reasons given in the rejection for Claim 34.

28. As per Claim 40, Miyachi teaches shifting storage locations at which row of image data is stored (c. 4, ll. 4-7).

However, Miyachi does not explicitly teach details of method for shifting rows, including second row address is determined by adding row offset value to first row address or subtracting row offset value from first row address. However, Choi teaches this, as discussed above for Claim 44. This would be obvious for the same reasons given in the rejection for Claim 38.

29. As per Claim 41, Miyachi does not explicitly teach that the control circuit provides a cyclic succession of row offset values to the logic unit. However, Choi discloses that the control

circuit provides a cyclic succession of row offset values to the logic unit [0036-0039]. This would be obvious for the same reasons given in the rejection for Claim 36.

Allowable Subject Matter

30. Claims 1-5 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

31. The prior art taken singly or in combination do not teach or suggest the combination of all of the limitations of Claim 1, especially the limitation of activating pixels of a screen line associated with a **new** row address based on the read stages of the row associated with the row address, and activating pixels of a screen line associated with a row address based on **new** states, where the read states are offset by a pixel position offset value, as recited in Claim 1.

32. The prior art also does not teach the combination of all of the limitations of Claim 2, especially the limitation of transmitting to the row driver a **new** address corresponding to the address of the read row offset by a first pixel position offset value, transmitting to a column driver **new** states corresponding to read states offset by the first pixel position offset value, as recited in Claim 2. Claims 3-5 depend from Claim 2 and therefore also contain allowable subject matter.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/

Supervisory Patent Examiner, Art Unit 2628